Optimization of the Al_2O_3/GaSb Interface and a High-Mobility GaSb pMOSFET

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***Abstract*—While there have been many demonstrations on n-channel metal–oxide–semiconductor field-effect transistors (MOSFETs) in III–V semiconductors showing excellent electron mobility and high drive currents, hole mobility in III–V p-channel MOSFETs (pMOSFETs) has traditionally lagged in comparison to silicon. GaSb is an attractive candidate for high-performance III–V pMOSFETs due to its high bulk hole mobility. We fabricate and study GaSb pMOSFETs with an atomic layer deposition Al_2O_3 gate dielectric and a self-aligned source/drain formed by ion implantation. The band offsets of Al_2O_3 on GaSb were measured using synchrotron radiation photoemission spectroscopy. The use of a forming gas anneal to passivate the dangling bonds in the bulk of the dielectric was demonstrated. The density of interface states D_{it} was measured across the GaSb band gap using conductance measurements, and a midband-gap D_{it} of $3 \times 10^{11}/cm^2eV$ was achieved. This enabled pMOSFETs with a peak hole mobility value of 290 cm^2/Vs.**

***Index Terms*—Atomic layer deposition (ALD), gallium antimonide, hole mobility, III–V p-channel metal–oxide–semiconductor field-effect transistors (pMOSFETs).**

I. Introduction

GaSb is an exciting III–V material, which may enable a high-performance/low-power complementary metal–oxide–semiconductor (CMOS) technology, which can outperform silicon. While there have been many demonstrations on n-channel metal–oxide–semiconductor field-effect transistors (nMOSFETs) in III–V showing excellent electron mobility and high drive currents, hole mobility in III–V p-channel MOSFETs (pMOSFETs) has traditionally lagged in comparison to silicon. GaSb is an attractive material for pMOSFET because of its high bulk mobility for holes ($\sim$850 cm^2/Vs), which is among the highest of all III–V semiconductors and twice as high as silicon and GaAs. The electron mobility in GaSb is five times higher, as compared with that in silicon. Another metric, which should be considered while comparing different semiconductors for CMOS applications, is the ratio of their electron mobility to hole mobility, which is proportional to the ratios of channel widths for the nMOSFET and pMOSFET to drive the same level of current. This ratio is $\sim$8 for GaSb, around 21 for GaAs, and greater than 50 for InAs and InSb. Thus, GaSb is more suited to enable a CMOS technology with traditional layout and circuit schemes.

GaSb also has other features that make it attractive for III–V CMOS. The charge neutrality level for GaSb is located at 0.1 eV from the valence band edge [1], thus the metal Fermi-level pins near the valence band for the metal/GaSb contact. This is favorable for obtaining contacts with low resistivity to p-type GaSb in the source/drain region of the pMOSFET. Contact resistivity values of less than 1×10^{-7} Ωcm^2 have been reported for p-type GaSb [2]. GaSb has a band gap of 0.72 eV, which is well matched to the loss minima for optical fiber communication and large enough to enable a high I_{ON}/I_{OFF} ratio, as compared to other III–V semiconductors [2]. Finally, GaSb has a melting point of 712 °C, as compared to 1238 °C for GaAs and 1414 °C for silicon. As for the thermal budget for processing scales with melting point, Sb-based materials are more suitable for low-temperature processing, which allows a simpler self-aligned process flow, and can be advantageously utilized when these materials are grown on top of another substrate, e.g., silicon, for heterogeneous integration.

The earliest attempt to fabricate MOSFETs on GaSb dates back to 1977 when Rockwell reported on a GaSb pMOSFET using pyrolytic silicon dioxide as the gate insulator [3]. The authors noted that the performance of the device was limited by the quality of the oxide, and the device showed a decrease in ON current and mobility with a decrease in measurement temperature indicating that the scattering mechanisms from the dielectric/interface were limiting the device performance. With the recent progress in the field of surface cleaning combined with atomic layer deposition (ALD), it has been possible to deposit high-quality dielectrics on III–V semiconductors. Many research groups have demonstrated nMOSFETs on an InGaAs/InP system using ALD dielectric and metal gate [4]–[6]. Only recently have people started investigating the passivation and interface properties of ALD oxide on GaSb [7], [8]. Ali *et al.* reported on the use of plasma-enhanced ALD to unpin the GaSb/dielectric interface [7]. Merckling *et al.*

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14. ABSTRACT

While there have been many demonstrations on n-channel metal?oxide?semiconductor field-effect transistors (MOSFETs) in III?V semiconductors showing excellent electron mobility and high drive currents, hole mobility in III?V p-channel MOSFETs (pMOSFETs) has traditionally lagged in comparison to silicon. GaSb is an attractive candidate for high-performance III?V pMOSFETs due to its high bulk hole mobility. We fabricate and study GaSb pMOSFETs with an atomic layer deposition Al2O3 gate dielectric and a self-aligned source/drain formed by ion implantation. The band offsets of Al2O3 on GaSb were measured using synchrotron radiation photoemission spectroscopy. The use of a forming gas anneal to passivate the dangling bonds in the bulk of the dielectric was demonstrated. The density of interface states Dit was measured across the GaSb band gap using conductance measurements, and a midband-gap Dit of 3 ?1011/cm2eV was achieved. This enabled pMOSFETs with a peak hole mobility value of 290 cm2/Vs.

15. SUBJECT TERMS
Atomic layer deposition (ALD), gallium antimonide, hole mobility, III?V p-channel metal?oxide?semiconductor field-effect transistors (pMOSFETs).

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explored the use of *in situ* deposition of Al_2O_3 on GaSb grown on InP using molecular beam epitaxy and reported D_{it} values in the low $10^{12}/cm^2eV$ range near the valence band [8]. While these are exciting results, the development of high-quality ALD dielectric on the GaSb surface still remains a nascent field, and MOSFETs on GaSb utilizing the ALD dielectric and their mobility have not been reported yet. In this paper, we explore the use of thermal ALD Al_2O_3 to achieve quality MOSFETs with a GaSb channel.

Another challenge in achieving high-performance MOSFETs on GaSb is the development of source/drain technology with high density of activated carriers, low defects, and low contact resistance. Ion implantation in antimonides has traditionally been a challenge; the formation of hillocks and voids has been well known with high-dose of ion implantation in GaSb [9], [10]. In this paper, we attempt to overcome these challenges and demonstrate a pMOSFET in GaSb substrate using ALD Al_2O_3 as the dielectric and source/drain formed by ion implantation in a self-aligned process flow.

The rest of this paper is organized as follows: In Section II, we report on the development of an Al_2O_3 gate dielectric on GaSb. Capacitance/conductance measurements and radiation from synchrotron are used to study the dielectric properties. The use of a forming gas anneal (FGA) to improve the dielectric properties is also discussed. Section III details the ion implantation process for forming source/drain and p^+/n diode characteristics for the pMOSFET. Section IV describes the fabrication flow and results obtained on the fabricated GaSb pMOSFET devices. Finally, we draw some conclusions in Section V.

II. Dielectric Development

A high-quality dielectric on the GaSb surface is the key for achieving good MOSFET characteristics. Here, we report on the optimization of ALD Al_2O_3 for the GaSb surface. We choose Al_2O_3 as it has the advantages of a large band gap, high dielectric constant, high breakdown field ($> 10^7$ V/cm), and thermal stability (amorphous for temperatures up to 1000 °C). The amorphous Al_2O_3 film also acts as a better barrier for alkali ions, has fewer impurities, and has higher radiation resistance. Any high-k oxide for a III–V MOSFET must satisfy two basic criteria, i.e., 1) a clean and native-oxide-free interface with the semiconductor and 2) sufficient band offset of over 1 eV to act as a barrier for both electrons and holes [1]. The GaSb surface has been known to be highly reactive to atmospheric oxygen, and a thick native oxide quickly forms on the surface [11]. The removal of this oxide to produce a clean and thermally stable surface is essential in achieving good interface quality and low density of interface states D_{it}. We use a chemical clean in 1:1 HCl for surface preparation before ALD. A HCl acid-based clean is effective to remove both the GaO_x and SbO_x on the GaSb surface. The comparison of various chemical cleans in producing a device-quality Sb surface was extensively studied using low-energy synchrotron radiation and photoluminescence measurements and has been reported elsewhere [12]. After the chemical clean, Al_2O_3 was deposited at 300 °C by ALD using trimethyl aluminum (TMA) and water as the precursors with TMA being the starting pulse for the ALD. The root-mean-square (RMS) roughness values of the surface just after HCl clean and after 10 cycles of ALD deposition were measured to be 0.66 and 0.73 nm, respectively, as shown in Fig. 1.

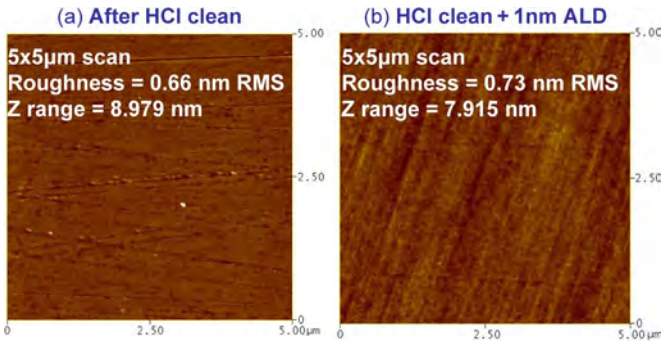

Fig. 1. AFM scan shows RMS roughness values of (a) 0.66 nm immediately after the chemical clean (b) and 0.73 nm after 10 cycles (∼1 nm) of Al_2O_3 deposited by ALD.

Synchrotron radiation photoemission spectroscopy (SRPES) was used to estimate the conduction band offset (CBO) and the valence band offset (VBO) for Al_2O_3 on GaSb. The Al_2O_3 band gap was measured to be 6.3 eV from the Al 2p loss spectrum [see Fig. 2(a)], which agrees well with values reported for ALD Al_2O_3 deposited under similar conditions [13]. The VBO was measured by taking the difference between the valence band spectrum from the surface after the clean and after thin Al_2O_3 deposition, as shown in Fig. 2(b) [14], using the Sb 4d peak from the GaSb substrate for alignment [see Fig. 2(c)]. The VBO was measured to be 3.1 eV by SRPES, which has a high-energy resolution near the valence band spectrum maximum. Using the known value of the GaSb band gap (0.72 eV) at room temperature, the CBO can be estimated by taking the difference of the Al_2O_3 band gap with the VBO and the GaSb band gap, as shown in Fig. 3. The measured CBO/VBO of 2.48 eV/3.1 eV for Al_2O_3 on GaSb are sufficient to minimize gate leakage by thermionic and tunneling processes, and the insulator is therefore well suited for a MOSFET design.

Al_2O_3 films with thicknesses of 5–15 nm were deposited on GaSb using ALD. Film thickness was measured using ellipsometry, which was also verified with cross-sectional transmission electron microscopy. Capacitors were made on these films using platinum (Pt) electrode deposited in an e-beam evaporator through a shadow mask. Fig. 4(a) plots the capacitance–voltage (CV) characteristics at 100 kHz for capacitors on p-type GaSb for varying thicknesses of as-deposited Al_2O_3. The capacitance values are normalized with respect to the maximum capacitance in accumulation to compare the shift in flatband voltage V_{FB}. We observe that in Fig. 4, the normalized capacitance curves are shifted parallel to each other for the as-deposited dielectric, indicating the presence of fixed charge in the bulk of the oxide and/or at the oxide/semiconductor interface. In addition, in comparison to the ideal V_{FB} value calculated using the effective work function of Pt on Al_2O_3 [15], the measured V_{FB} is negatively shifted with respect to the ideal value for the thinner oxide thickness, whereas a positive V_{FB} shift is observed for thicker dielectric thicknesses with respect to the ideal value.

This issue is further examined in Fig. 5, where V_{FB} is plotted as a function of oxide thickness for the as-deposited dielectric.

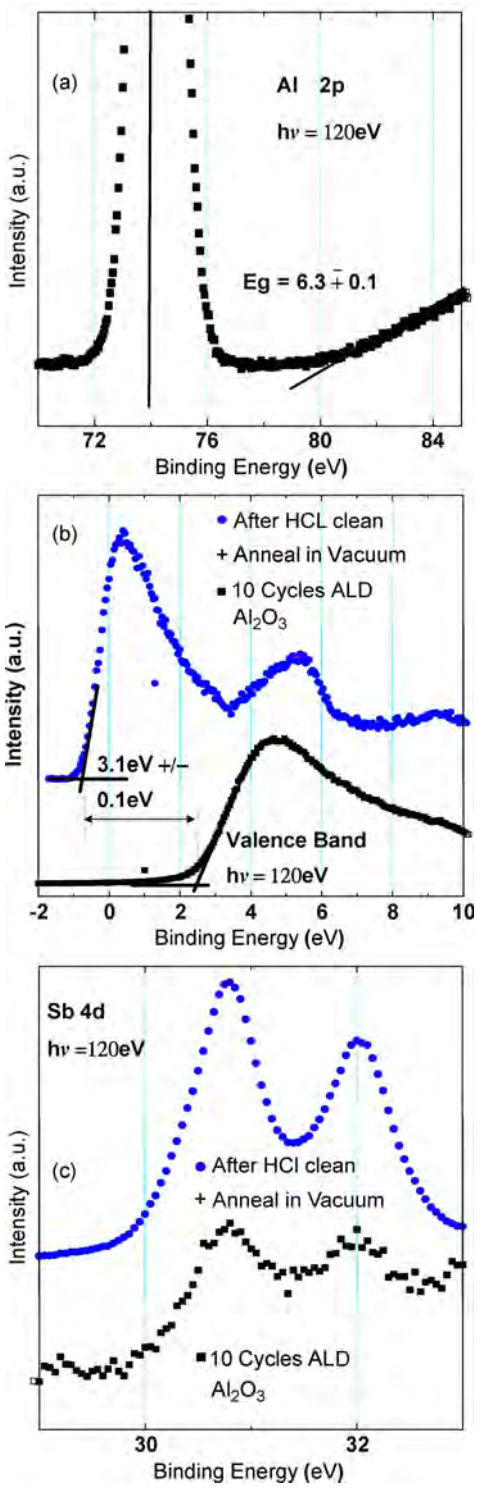

Fig. 2. (a) Band gap E_g of Al_2O_3 is measured using the Al 2p loss spectrum. (b) VBO is measured by taking the difference between the valence spectrum before and after depositing a thin layer of Al_2O_3. (c) While using the Sb 4d peak from the substrate for alignment.

V_{FB} was extracted using the method of Hillard *et al.* [16]. The observed thickness dependence of V_{FB} can be explained if we assume that there is negative fixed charge near the Al_2O_3 interface with GaSb and positive charge in the bulk of the oxide film. A negative linear shift in V_{FB} as a function of dielectric thickness occurs due to negative charge at the semiconductor/oxide interface, as shown in Fig. 5, whereas a positive parabolic shift is expected when there is positive bulk charge present in the dielectric [17]. The functional dependence of the measured data can be fitted very well with the combination of negative linear and positive parabolic dependence (see Fig. 5), confirming the presence of positive bulk charge in the oxide and negative charge at the oxide/GaSb interface for the as-deposited Al_2O_3. A similar charge distribution has been also observed for Al_2O_3 on InGaAs deposited under similar conditions by Shin *et al.* [18]. The authors attributed this charge distribution to the presence of an O-rich region near the interface and an Al-rich region away from the interface. It is known from first-principle calculations in amorphous Al_2O_3 that the Al deficiency manifests itself in the form of oxygen dangling bonds,

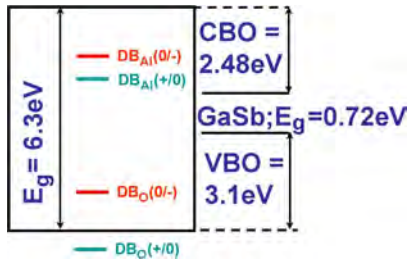

Fig. 3. Band offsets for Al_2O_3 deposited by ALD on GaSb. The position of charge transition levels for dangling bonds in the oxide has been overlayed with the band diagram of the oxide.

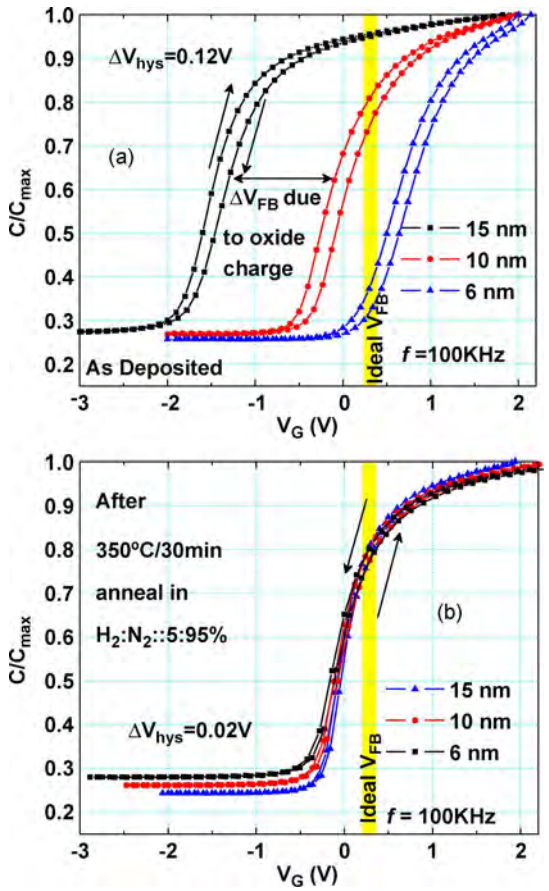

Fig. 4. High-frequency CV characteristics on (a) as-deposited Al_2O_3 and (b) after FGA. The capacitance values are normalized to compare the V_{FB} shift with varying dielectric thicknesses.

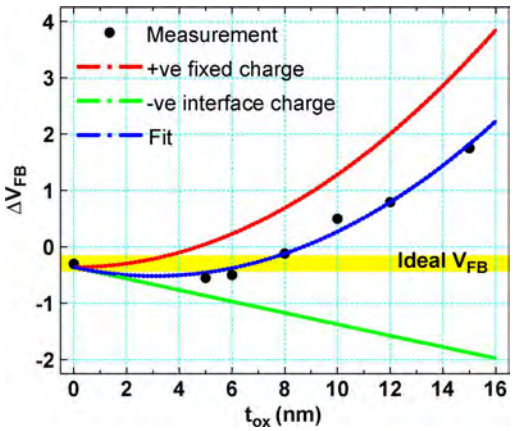

Fig. 5. Measured $V_{\rm FB}$ shift as a function of physical oxide thickness $t_{\rm ox}$. Experimental data can be fitted very well combining a linear shift with $t_{\rm ox}$ due to negative interface charge and a parabolic shift with $t_{\rm ox}$ due to positive bulk charge.

which have charge-transition levels at -0.83 and 0.61 eV above the valence band, as shown in Fig. 3, whereas the aluminum dangling bonds due to O deficiency are located at 5.12 and 5.35 eV above the valence band (see Fig. 3) [18]. Looking at the position of these dangling bonds in Fig. 3, we can predict that the O dangling bonds will be below the Fermi level and thus will be negatively charged, whereas the Al dangling bonds will be positively charged. This agrees well with the experimental result that the O-rich region near the interface has fixed negative charge, whereas the Al-rich region in the bulk has positive charge.

As the presence of fixed charge in the oxide or at the oxide/semiconductor is detrimental for MOSFET performance, the use of FGA was explored to reduce the fixed charge and improve the Al_2O_3/GaSb interface properties. Recently, the use of FGA has been shown to be very effective at improving the interface properties of the oxide/$In_xGa_{1-x}As$ interface and passivating the bulk traps in Al_2O_3 deposited by ALD under similar conditions [18], [19]. A theoretical analysis has predicted binding energy values of 1.3 eV for O–H and 1.4 eV for Al–H indicative of stable passivation. Hydrogen passivation can hence neutralize the effect of dangling bonds and improve the interface properties. Motivated by this, we tried an FGA anneal with forming gas $(5/95\% : H_2/N_2)$ flowing at the rate of $\sim$4 L/min at varying temperatures. A 30 min/350 °C anneal was found to be optimum to improve the dielectric properties. Fig. 4(b) plots the CV characteristics following the FGA anneal, where the normalized CVs for different dielectric thicknesses overlap each other, indicating the removal of fixed charge. The hysteresis reduces from $\sim$120 mV for the as-deposited condition to $\sim$20 mV after the FGA anneal, indicating passivation of bulk traps (see Fig. 4). A reduction in stretch-out indicating reduction of $D_{\rm it}$ was also observed. The temperatures above and below 350 °C were found to be less effective in improving the dielectric properties with FGA. A similar behavior with temperature has been observed with the effect of FGA on the dielectric/Ge interface [20] and has been attributed to insufficient diffusion of hydrogen radicals at low temperatures $(< 350\ ^\circ\text{C})$ and deterioration of interface properties due to intermixing at the semiconductor/dielectric interface and desorption of hydrogen at higher temperatures $(> 350\ ^\circ\text{C})$.

Fig. 6 plots the CV characteristics obtained after the FGA anneal on p- and n-type GaSb substrates for the frequency range of 1–100 kHz. An inversion response at room temperature was observed on both n- and p-type GaSb substrates. Frequency dispersion in accumulation, which is one indicator of $D_{\rm it}$, was less than 1/2.1%/dec for the p- and n-type substrates. The $D_{\rm it}$ distribution across the band gap was determined using the conductance method in the depletion region [21], [22] on n- and p-type substrates. The temperature was varied from 300 K–80 K, and measurements were made on both n- and p-type substrates to probe the $D_{\rm it}$ distribution across the entire band gap. Fig. 7 shows a typical G_p/ω versus frequency curve for the p-type substrate at 77 K. Fig. 8 plots the derived $D_{\rm it}$ distribution. A midband-gap $D_{\rm it}$ value of $3 \times 10^{11}/\text{cm}^2\text{eV}$ was achieved. The $D_{\rm it}$ distribution is asymmetric with low $D_{\rm it}$ near the valence band edge and an order of magnitude higher $D_{\rm it}$ toward the conduction band. The low $D_{\rm it}$ values near the valence band is encouraging for obtaining a good pMOSFET, whereas the high $D_{\rm it}$ values near the conduction band can be detrimental to the nMOSFET performance. It must be noted that the minimum of the $D_{\rm it}$ distribution occurs near the charge neutrality level of GaSb, which is located at $\sim$0.1 eV from the valence band [1]. We also note that the $D_{\rm it}$ distribution obtained is qualitatively similar to what is experimentally observed in germanium, which has a similar band gap as GaSb, and its charge neutrality center is located near the valence band as well [23].

III. Diode Development for Source/Drain

For the development of GaSb pMOSFET source/drain technology with a high density of activated carriers, low defects and low contact resistance are essential. Ion implantation in the antimonides has traditionally been a challenge, as the formation of hillocks and voids with a high dose of implantation in GaSb has been well known [9], [10]. In addition, it has been reported that this damage does not go away with furnace or rapid thermal anneal (RTA) even at high temperature. Furthermore, it has been noted that the threshold dose/energy of hillock formation decreases with increasing ion mass [9], [10]. Table I lists the dopant species for GaSb, i.e., Be, Si, and Zn act as acceptors in GaSb, and S, Se, and Te are the common donors. Thus, for the p^+/n diode, the implantation dose at which hillock formation occurs is on the order of Zn $<$ Si $<$ Be. Similarly, for the n^+/p diode, it is on the order of S $<$ Se $<$ Te. The problem is worse for donors as the lightest atom for donors is S compared to Be for acceptors. It should be also noted that most of the previous work on implantation in GaSb was done without any dielectric layer on the top to absorb the energy of species being implanted.

We experimented with ion implantation of several species in GaSb using thin ($\sim$10 nm) Al_2O_3 as the capping layer. The selection of implant energy and dose was guided by simulations performed with SRIM software [24] to produce a peak of the dopant species at the surface. Fig. 9(a)–(c) shows the atomic force microscopy (AFM) map of the surface after implantation

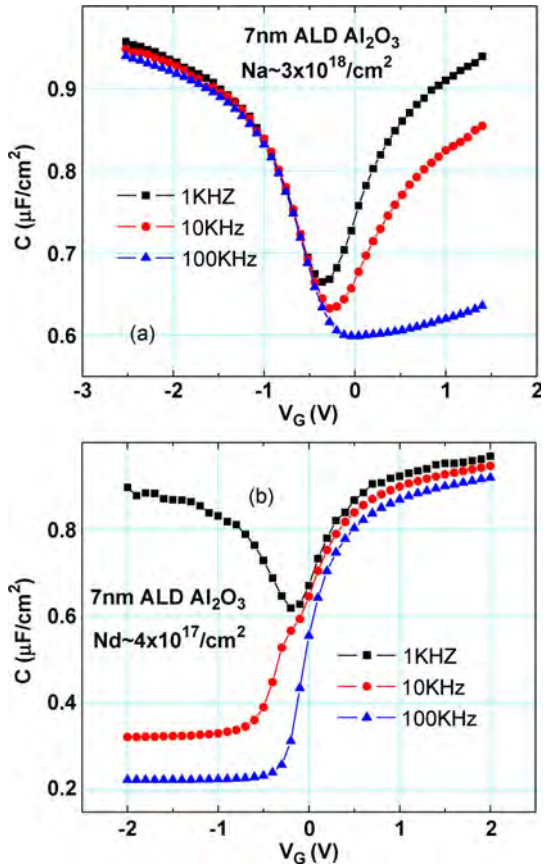

Fig. 6. Measured CV characteristics at room temperature over a frequency range of 1–100 kHz on (a) p-type GaSb with Na $\sim 3 \times 10^{18}/\text{cm}^2$ (b) n-type GaSb with Nd $\sim 4 \times 10^{17}/\text{cm}^2$.

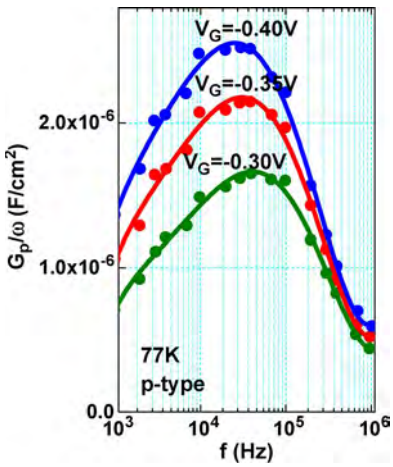

Fig. 7. Measured parallel G/ω as a function of frequency for various gate voltages measured on a p-type GaSb capacitor at 77 K.

with Be, S, and Zn, respectively. A significant increase in surface roughness due to implant damage was observed for heavier species such as S and Zn. Furthermore, we observed that the surface still remains rough after RTA [see Fig. 9(d)]. The only good result was on Be, which has the lowest atomic mass and for which the surface roughness was less than 1 nm for an implant dose of $9 \times 10^{14}/\text{cm}^2$. Various implant and anneal conditions were attempted for Be to optimize the p^+/n diode characteristics for the pMOSFET. The obtained diode IV

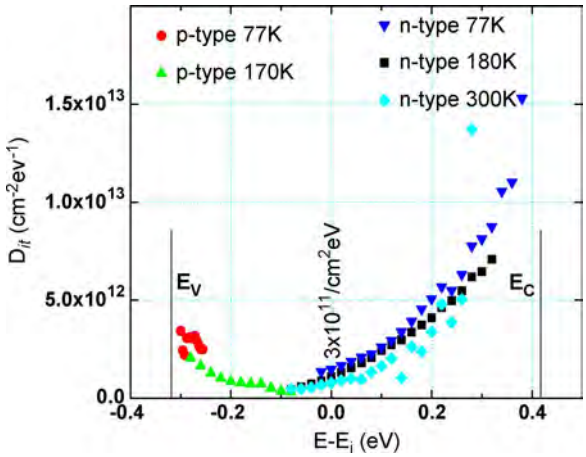

Fig. 8. D_{it} distribution is calculated across the band gap using the conductance method. D_{it} is scanned across the band gap utilizing both the p- and n-type substrates and varying the measurement temperature from 300 K to 77 K.

TABLE I
DOPANT SPECIES IN GaSb

Name	Nature	Atomic Mass
Be	Acceptor	9
Si	Acceptor	28
Zn	Acceptor	65.4
S	Donor	32
Se	Donor	78.9
Te	Donor	127.6

characteristics are plotted in Fig. 10(a). Good diode characteristics with $I_{\text{ON}}/I_{\text{OFF}}$ of $> 5 \times 10^4$ and an ideality factor of 1.4 could be obtained with annealing at 350 °C, as shown in Fig. 10(b).

Fig. 11 plots the temperature dependence of the reverse leakage current for the p^+/n diode. Reduction in reverse current was observed when the temperature was decreased from 300 K to 80 K. Activation energy E_a was calculated to be ~0.33 eV from the slope of the observed characteristics in Fig. 11. This value is close to half of the band gap of GaSb ($E_g \sim 0.72$ eV), suggesting that the intrinsic generation–recombination is dominant in the reverse leakage current [17], [25], [26].

IV. TRANSISTOR FABRICATION AND CHARACTERISTICS

GaSb pMOSFETs were fabricated using a self-aligned gate-first process flow on an n-type GaSb substrate grown by the Czochralski process with Te as the n-type dopant. A carrier concentration of ~ 3–$4 \times 10^{17}/\text{cm}^3$, which was the lowest available commercially, was chosen to reduce the effect of Coulomb scattering on transistor mobility. One hundred cycles (~10 nm) of ALD Al_2O_3 were deposited at 300 °C for use as the gate dielectric, followed by evaporation and patterning of the aluminum gate material. This was followed by ion implantation of beryllium. The source and drain contacts were formed by Ti/Ni

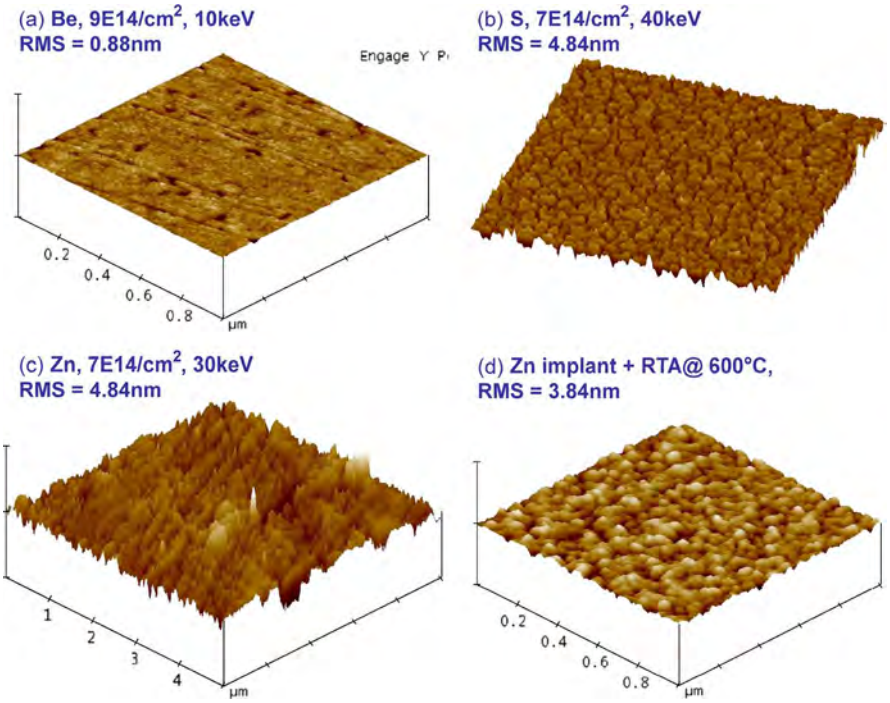

Fig. 9. AFM scan of the surface after: (a) Be implant with dose $= 9 \times 10^{14}/\text{cm}^2$ and energy $= 10$ keV; (b) S implant with dose $= 7 \times 10^{14}/\text{cm}^2$ and energy $=$ 40 keV; (c) Zn implant with dose $= 7 \times 10^{14}/\text{cm}^2$ and energy $= 30$ keV; and (d) RTA anneal of the Zn implanted sample at 600 °C for 5 min.

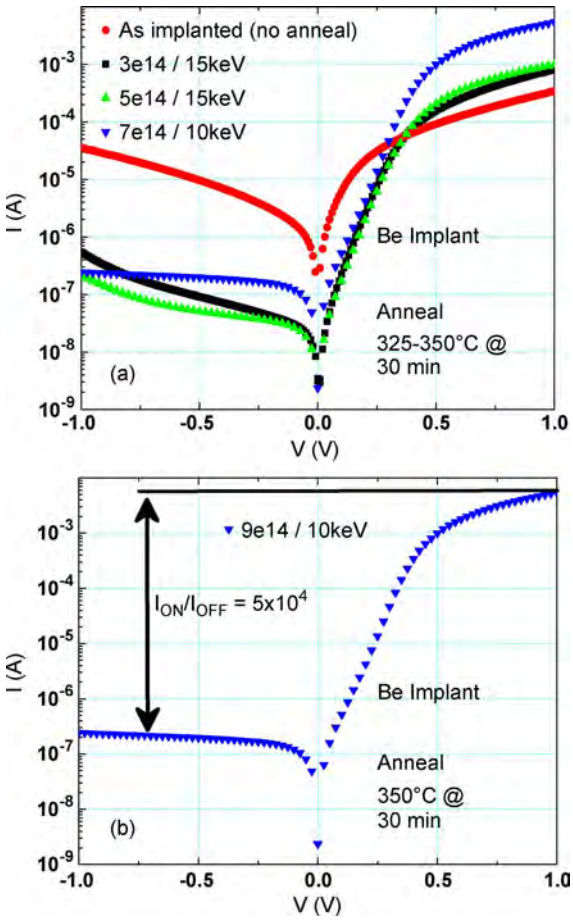

Fig. 10. (a) Various implant and anneal conditions were attempted to optimize the diode characteristics. (b) Diode with $I_{\text{ON}}/I_{\text{OFF}}$ of 5×10^4, and ideality factor of 1.4 was achieved with annealing at 350 °C.

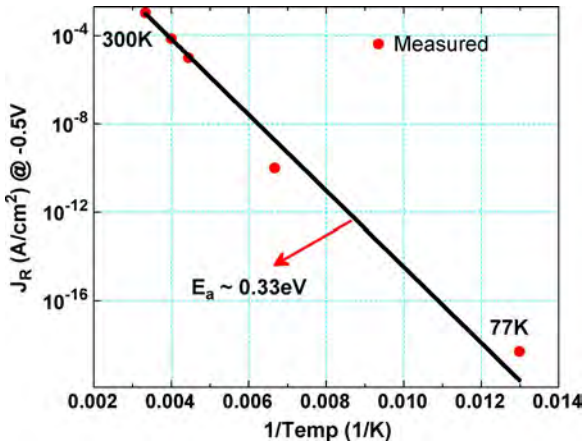

Fig. 11. Reverse current J_R at applied voltage of -0.5 V is measured as a function of temperature. The activation energy E_a of 0.33 eV is extracted from the slope.

deposition and liftoff. Fabrication of the transistors was completed with a 350 °C forming gas anneal, which also activates the source/drain implant. The temperature during the entire process never exceeds 400 °C. The low temperature required for source/drain activation allows for a self-aligned gate-first process flow without causing intermixing at the $Al_2O_3/GaSb$ interface. The sheet resistance in the source/drain regions was measured to be 300 Ω/square using the transfer length method. Specific contact resistance of the Ti/Ni source/drain contact was measured to be $\sim 2 \times 10^{-5}$ Ωcm^2.

Fig. 12 plots the I_D–V_G characteristics for the MOSFET device. The source current ON/OFF ratio is $> 10^4$, whereas the off current for the drain is limited by the reverse leakage through the large drain/body contact at large drain voltages (see

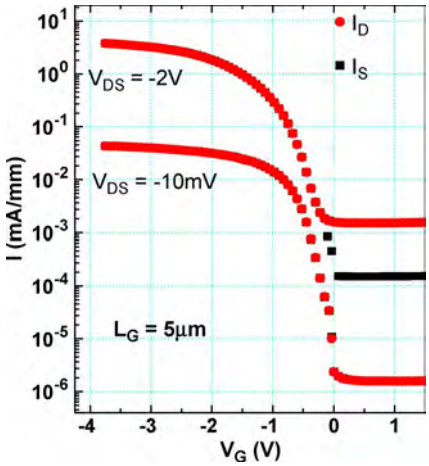

Fig. 12. Output characteristics of the GaSb pMOSFET.

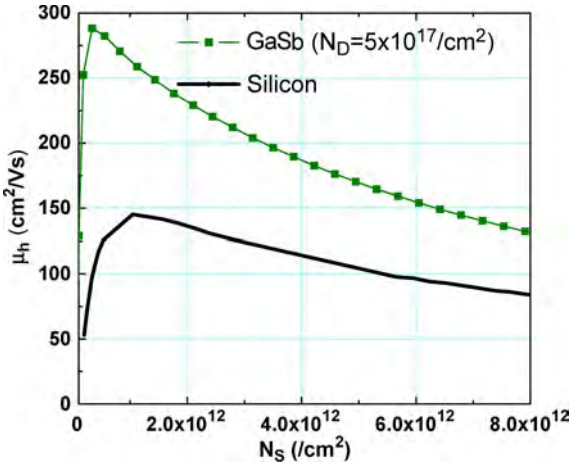

Fig. 13. Hole mobility as a function of sheet charge. Silicon universal hole mobility data are plotted for comparison. Peak hole mobility of 290 $\mathrm{cm}^2/\mathrm{Vs}$ was obtained.

Fig. 12). The mobility for these transistors was extracted using the split CV analysis based on the I_D–V_G characteristics of the transistors (gate length $= 25\ \mu\mathrm{m}$) and the gate-to-channel capacitance C_{GC} measured at 100 kHz [17]. Note that no corrections for source/drain resistance or any other corrections were applied while extracting the mobility. Fig. 13 plots the extracted mobility as a function of sheet charge in the channel; a peak field-effect hole mobility of 290 $\mathrm{cm}^2/\mathrm{Vs}$ was obtained. Universal hole mobility in silicon is also plotted for comparison (see Fig. 13); the peak mobility in GaSb MOSFET is approximately twice higher in comparison to silicon, and the mobility gain over silicon is maintained even at high sheet charge. An increase in the ON current and correspondingly the mobility was observed when the temperature was decreased from 300 K to 80 K. The temperature dependence of mobility at a fixed sheet charge density of $5 \times 10^{12}/\mathrm{cm}^2$ is plotted in Fig. 14. The temperature dependence of $T^{-0.85}$ is observed, which is closer to the $T^{-1.0}$ dependence associated with mobility limited by interface roughness scattering. We did observe higher roughness in our devices, as compared to silicon/germanium from the AFM study in Fig. 1. The surface roughness on the GaSb surface clean was 0.66 nm, which is roughly twice higher in comparison to state-of-art silicon [27]. We believe that further optimization of the transistor output characteristics is possible with further improvement of the diode characteristics using a higher implant dose and an RTA.

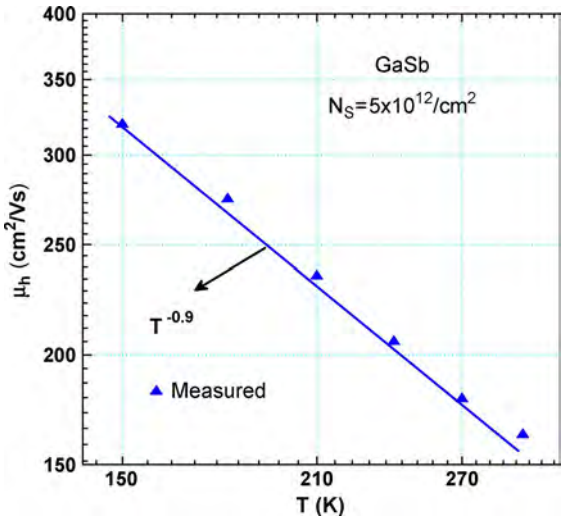

Fig. 14. Temperature dependence of hole mobility is plotted at fixed sheet charge of $5 \times 10^{12}/\mathrm{cm}^2$.

V. Conclusion

In conclusion, we have reported on the development of a high-quality ALD Al_2O_3 gate dielectric on GaSb. The band offsets of Al_2O_3 on GaSb were measured using SRPES and determined to be suitable for MOSFET development. FGA was effectively used to passivate the dangling bonds in the bulk of the dielectric and also to improve the interface properties [18]–[20]. Excellent CV characteristics were demonstrated on both p- and n-type substrates with frequency dispersion of less than 1/2.1%/dec. The D_{it} distribution was measured across the GaSb band gap using conductance measurements; midband-gap D_{it} of $3 \times 10^{11}/\mathrm{cm}^2\mathrm{eV}$ was achieved. A p^+/n diode with an ON/OFF ratio of 5×10^4 and an ideality factor of 1.4 was demonstrated using ion implantation of Be.

A self-aligned process flow was used for fabricating pMOSFETs with the source/drain formed by ion implantation of Be. The maximum temperature during the process flow does not exceed 400 °C. Good transistor characteristics with $I_{\mathrm{ON}}/I_{\mathrm{OFF}} > 10^3$ and peak hole mobility of 290 $\mathrm{cm}^2/\mathrm{Vs}$ were obtained. Temperature-dependent measurements revealed a mobility value limited by interface scattering and a defect-free diode. This development paves the way for the demonstration of a complementary technology in III–V materials outperforming silicon.

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